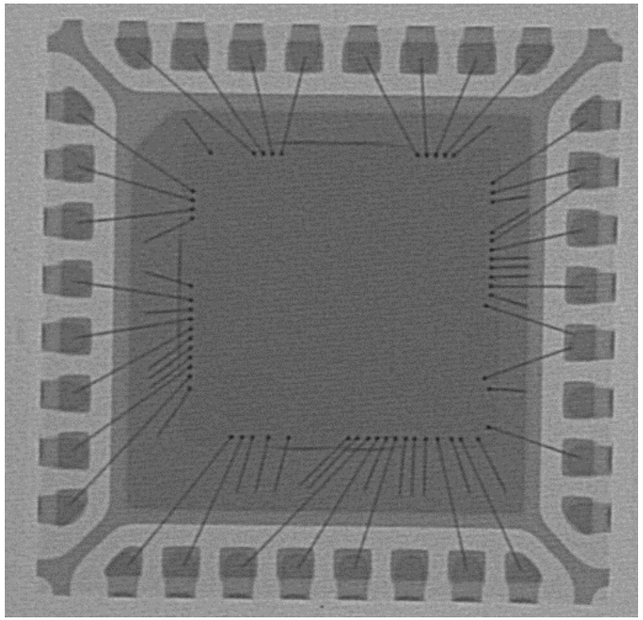
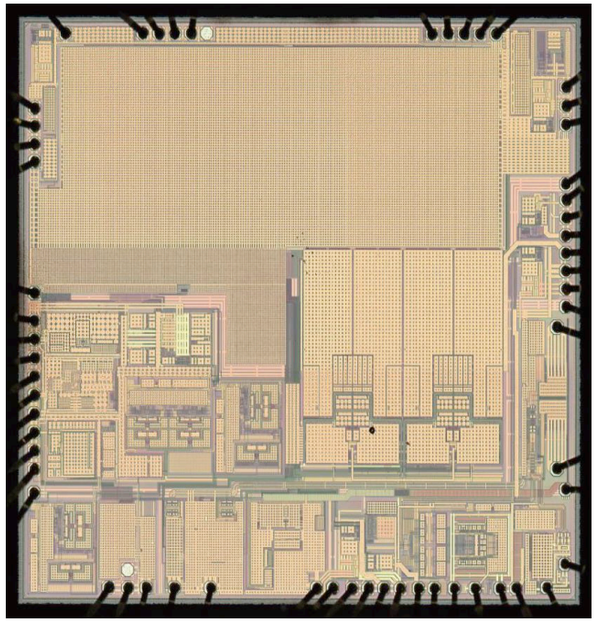
Exhibit B

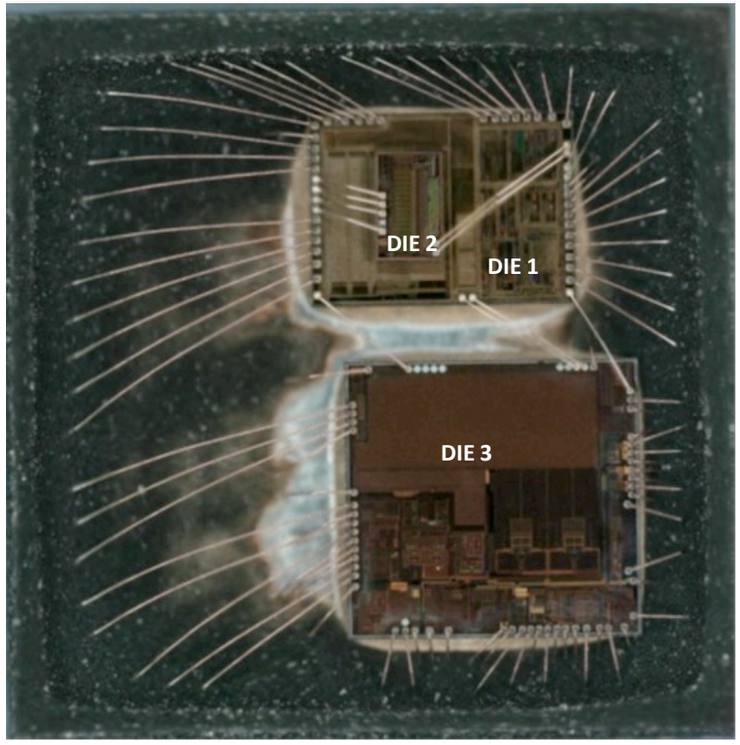
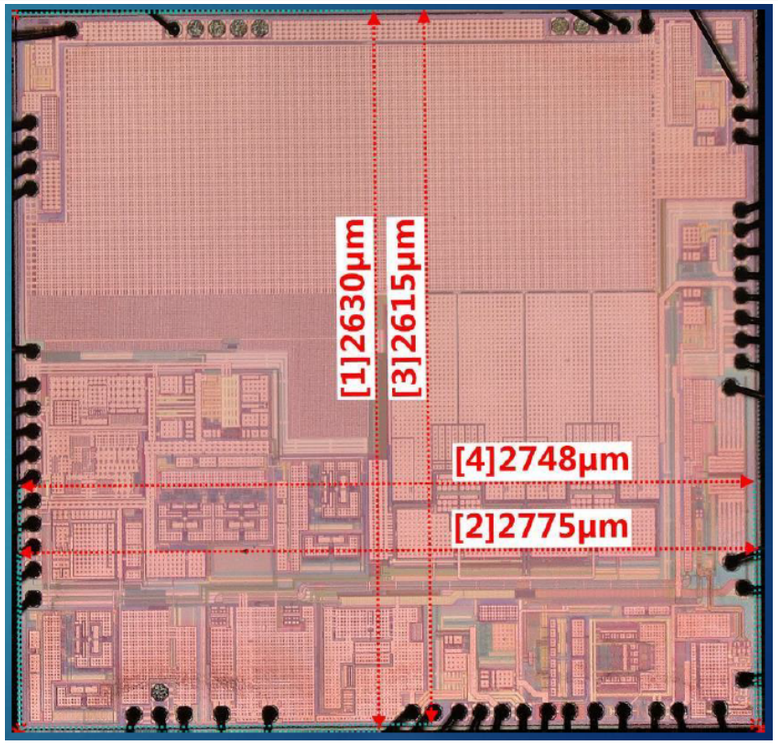
to

Beken's Complaint for Patent Infringement

Claim Chart for the '228 Patent

US Patent No. 9,197,228 Exemplary Claim 9[1]	**Mapped against Auctus Technology AT1846S chip**	
9. A method comprising:	**X-Ray Photo of the Auctus's AT1846S chip:**  **Top view of the AT1846S chip:**  In the X-Ray Photo, the black lines are bonding wires, connecting the die pad with chip pins. **Photo of the chip A21 of the patent claims** **Top view of the Auctus's AT1846S chip with measurements:**	

[1] Beken provides this exemplary claim chart for the purposes showing one basis of infringement of the '228 Patent by the Accused Products as defined in the Complaint at ¶27. This exemplary claim chart addresses the Accused Products broadly based on the fact that the Accused Products infringe in the same general way. Beken reserves its right to amend and fully provide its infringement arguments and evidence thereof until its Infringement Contentions are later produced according to the court's Scheduling Order in this case.

	  The above two photos indicate the chip encapsulation of the AT1846S chip completely overlaps with the encapsulation of chip A21 in terms of the component layout and size.	
generating an oscillating signal (Fvco) by an oscillator;	In the Programming Guide of the AT1846S chip, a frequency synthesizer (oscillator) generates an oscillating signal. (Both frequency synthesizer and oscillator are frequency generator sources that generates frequency output, such as the oscillator signal in the patent claims).	

	3.3 Synthesizer The frequency synthesizer generates the local oscillator signal. All building blocks are fully integrated without any external components. LO frequency can be programmed through the serial interface by the MCU. *(How to select frequency band and program LO frequency, refer to the programming guide)*	

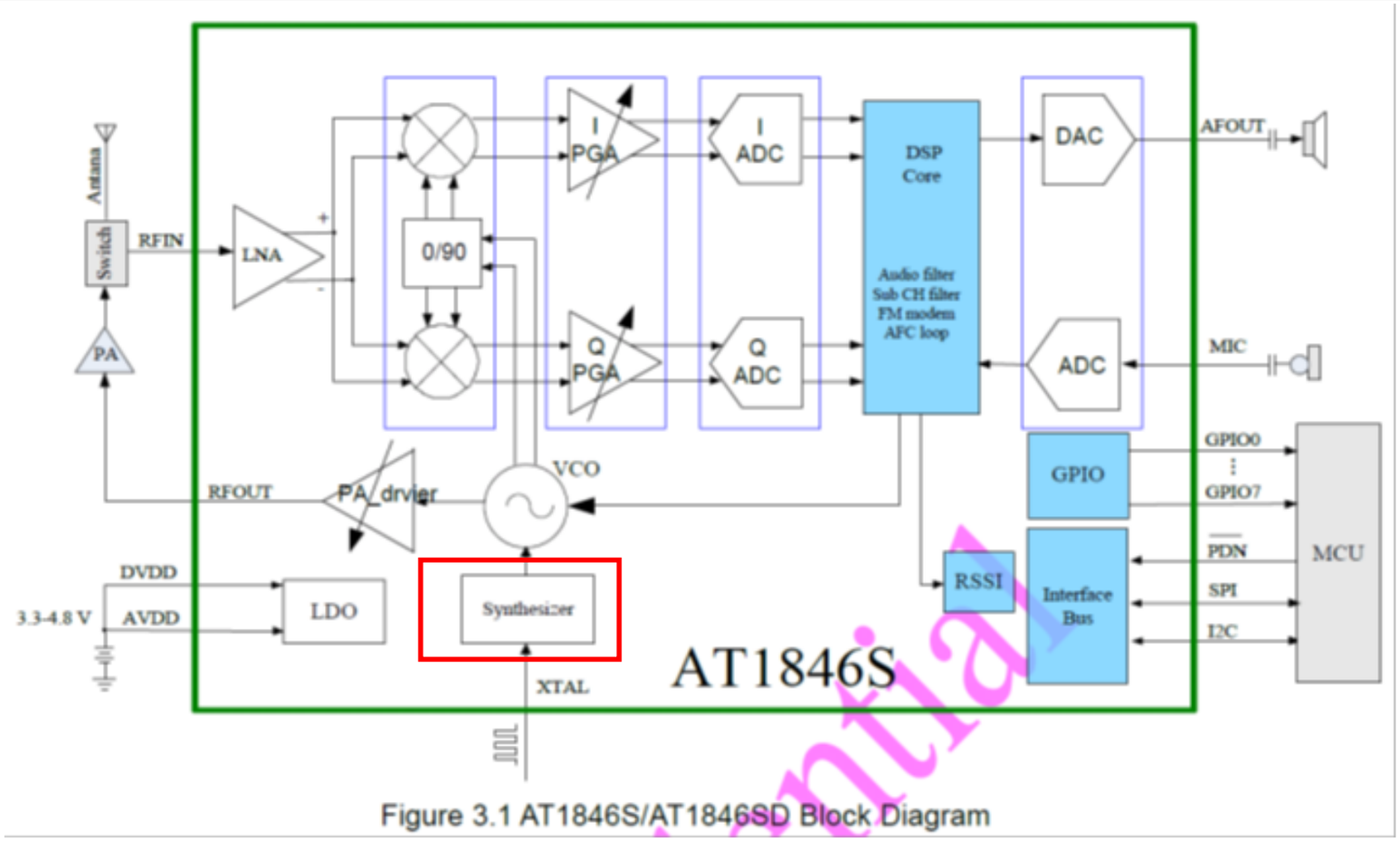


Figure 3.1 AT1846S/AT1846SD Block Diagram

In the Programming Guide of the AT1846S chip, as shown below, the chip supports a specific range of frequency signals, further indicating an oscillator signal is generated and adjusted by the AT1846S chip.

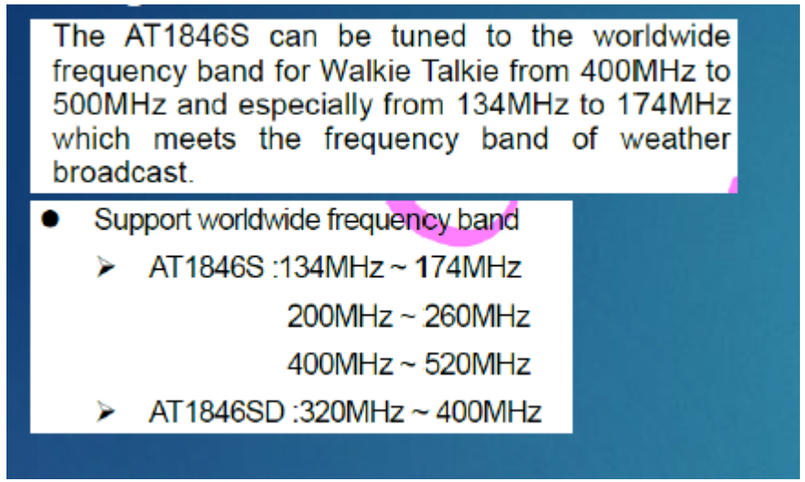


Table 5-1 Receiver Characteristics

(AVDD = 3.3 V, TA = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Fin	Input Frequency Range1	AT1846S	400		520	MHz
	Input Frequency Range2	AT1846S	134		174	MHz
	Input Frequency Range3	AT1846S	200		260	MHz
	Input Frequency Range4	AT1846SD	320		400	MHz

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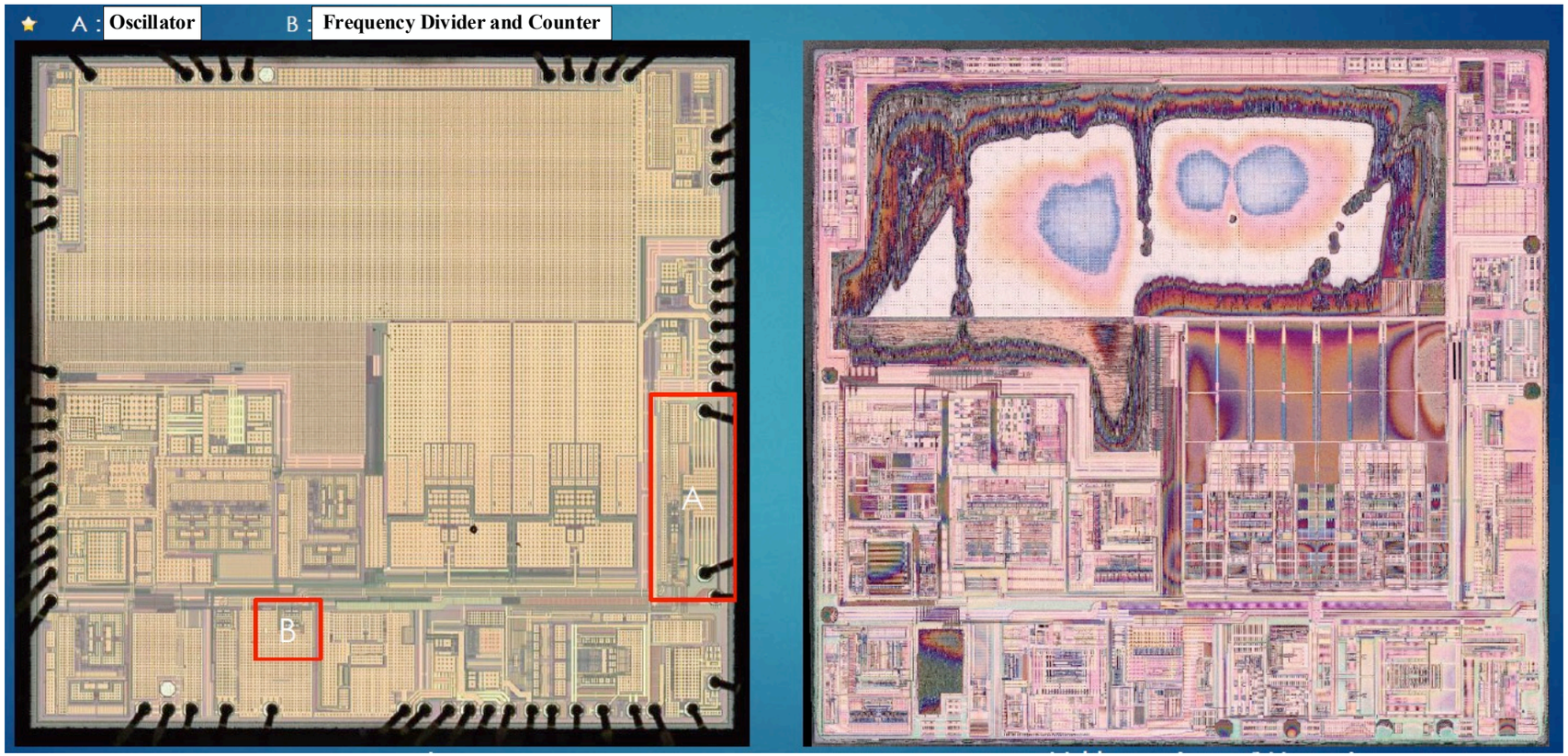
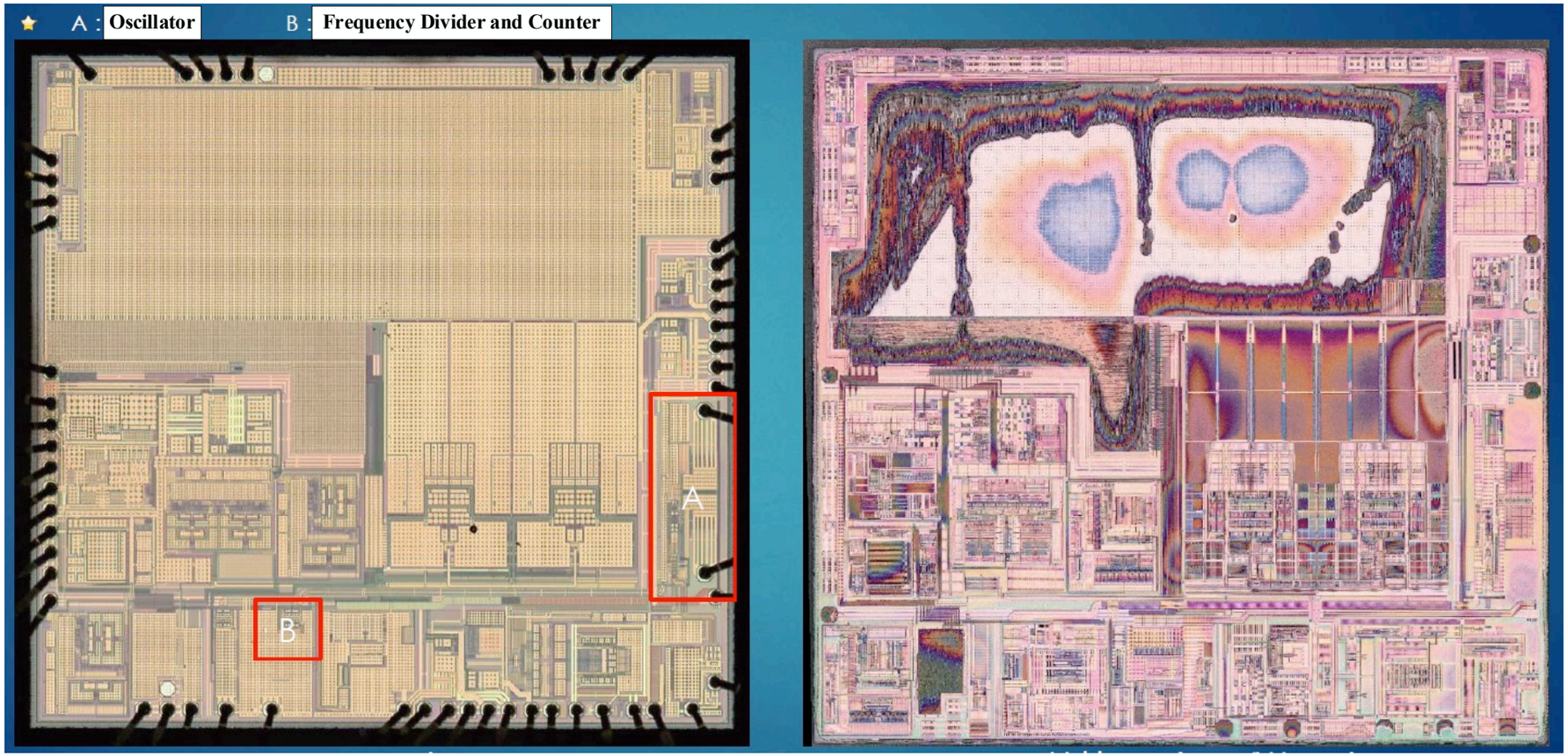
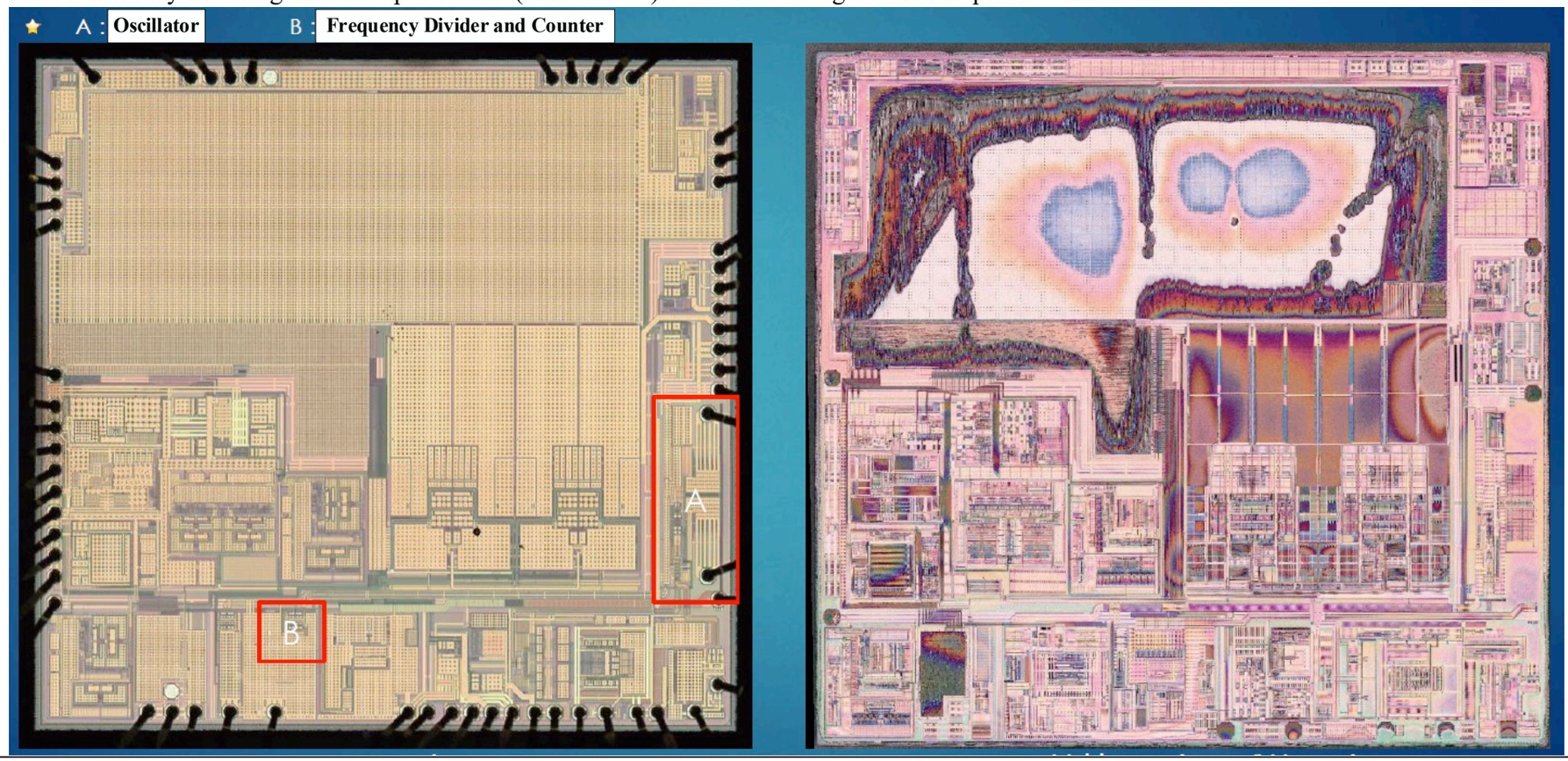
Further, as shown below, block A in the picture to the left indicates the location where the oscillator resides on the AT1846S chip. The picture to the right shows a photo of the AT1846S chip with three metal layers removed. Metal layers are typically applied to chips to provide required signal crossings and power supply rails. Without the metal layers, the layout of the circuit underneath is revealed to a greater extent.

	Therefore, the AT1846S chip includes an oscillator that generates oscillating signals. 	
generating a divided signal by dividing a	As shown below, block B in the picture to the left indicates where a frequency divider and a counter reside on the AT1846S chip. The picture to the right shows a photo of the AT1846S chip with three metal layers removed. The frequency divider in the corresponding section is revealed in greater detail without the metal layers.	

frequency of the oscillating signal by a denominator;	 Therefore, the AT1846S chip includes a frequency divider that generates a divided signal by dividing the frequency of the oscillating signal. A frequency divider generates an output frequency signal by dividing the input frequency signal with an integer as a denominator, e.g., $f_{out}=f_{in}/n$. Therefore, the denominator recited in the claims is inherently required.

obtaining a first count of the divided signal (Fvco/N) within a predetermined time and a second count of a reference signal within the predetermined time;	As shown below, in the picture to the left, block B indicates where a frequency divider and a counter reside on the AT1846S chip. The picture to the right shows a photo of the AT1846S chip with three metal layers removed. The counter in the corresponding section is revealed in greater detail without the metal layers. The counter may be configured to output a count ("first count") of the divided signal within a predetermined time. 	

A reference signal is generated by a reference circuit. A reference circuit is inherent to chips. Thereby, the counter may be configured to output a count (e.g., second count) of the reference signal within the predetermined time.

The existence of the reference circuit may be further evidenced based on the discussion of a master reference clock in the Programming Guide of the AT1846S chip, as shown below, which inherently generates a reference signal.

2. Reference Clock

AT1846S/AT1846SD takes 12.8 MHz,13MHz,25.6M Hz and 26MHz crystals as its master reference clock.

Bit	Name	Function
30H[14]	xtal_mode	1: 26MHz/13MHz 0: 25.6MHz/12.8MHz
04H[0]	clk_mode	1: 12.8MHz /13MHz 0: 25.6MHz /26MHz

For example: 12.8MHz crystal

04H[0]= clk_mode =1

30H[14]= clk_mode =0

13MHz crystal

04H[0]= clk_mode =1

30H[14]= clk_mode =1

26MHz crystal

04H[0]= clk_mode =0

30H[14]= clk_mode =1

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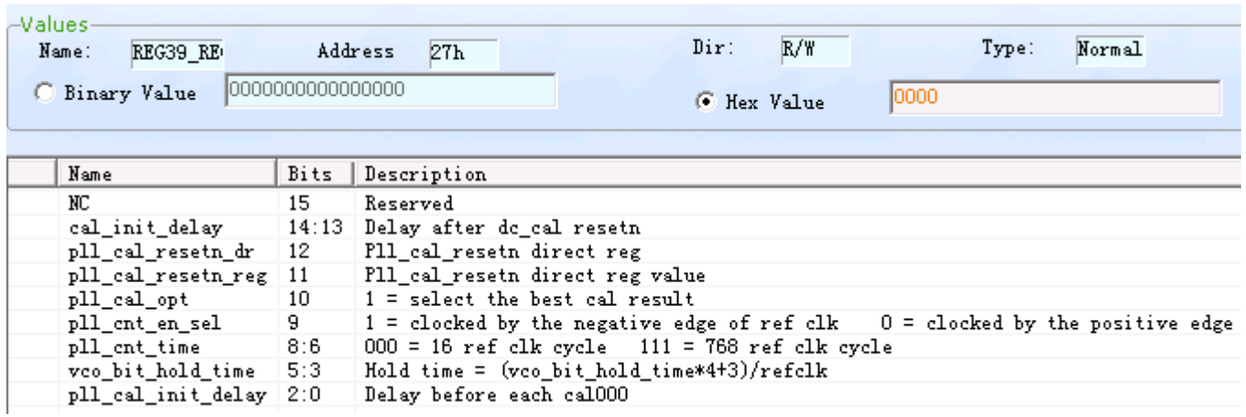
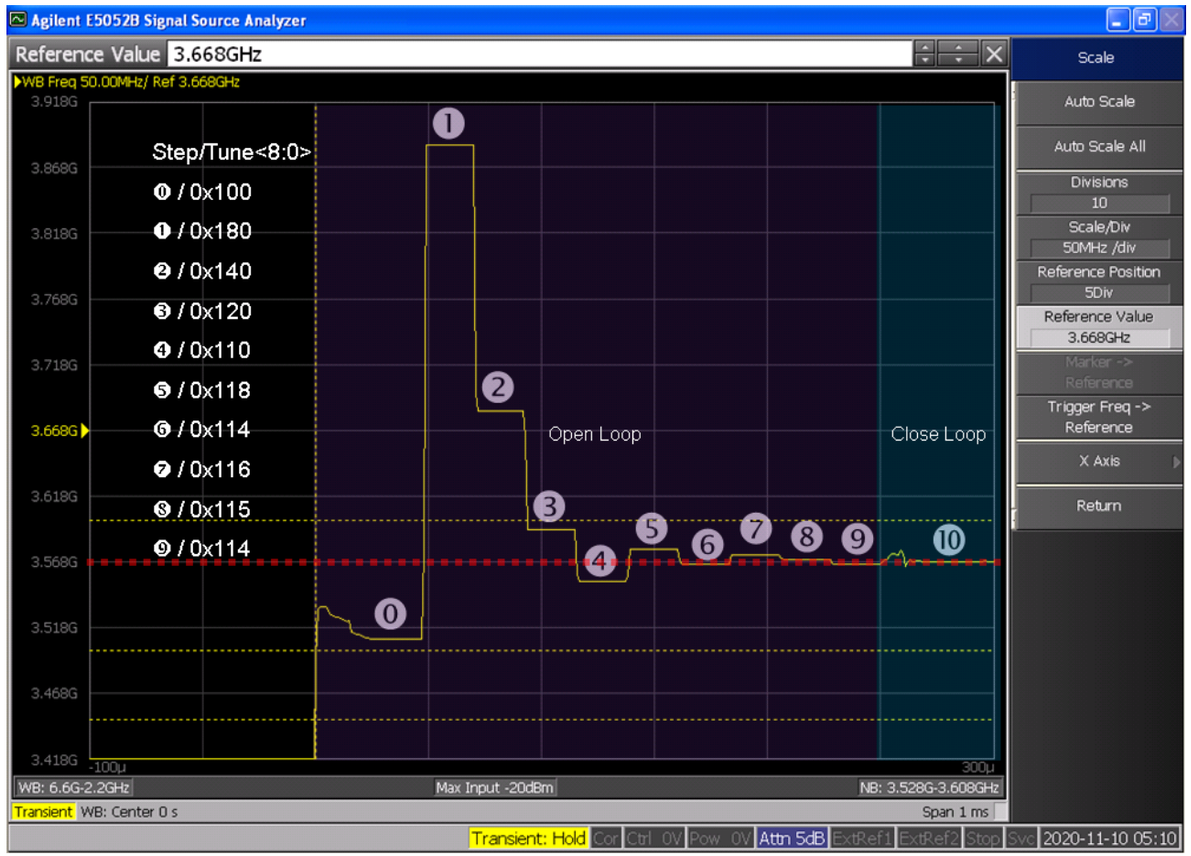
	The use of "predetermined time" and a reference circuit is further evidenced based on the below information acquired by testing the AT1846S chip. Specifically, the use of reference signal generated by a reference circuit may be indicated by the "negative edge of ref clk" and the "positive edge" of the reference clock. The use of "predetermined time" for at least the second count of the reference signal may be indicated by "pll_cnt_time," referring to the "ref clk cycle" (i.e., reference clock cycle).  Values Name: REG39_RE Address 27h Dir: R/W Type: Normal Binary Value 0000000000000000 Hex Value 0000 Name | Bits | Description NC | 15 | Reserved cal_init_delay | 14:13 | Delay after dc_cal resetn pll_cal_resetn_dr | 12 | Pll_cal_resetn direct reg pll_cal_resetn_reg | 11 | Pll_cal_resetn direct reg value pll_cal_opt | 10 | 1 = select the best cal result pll_cnt_en_sel | 9 | 1 = clocked by the negative edge of ref clk 0 = clocked by the positive edge pll_cnt_time | 8:6 | 000 = 16 ref clk cycle 111 = 768 ref clk cycle vco_bit_hold_time | 5:3 | Hold time = (vco_bit_hold_time*4+3)/refclk pll_cal_init_delay | 2:0 | Delay before each cal000	
generating a comparison result according to a comparison of the first count	A comparator is utilized in the AT1846S chip to generate a comparison result according to a comparison of the first count of the divided signal and the second count of a reference signal. The existence of a comparator may be inferred by testing digital signals in the chip. For example, an aging calibration curve generated by digital signals may be analyzed to infer the existence of a comparator.	

and the second count;	The screenshot below shows a curve indicating the changes of VCO (Voltage-Controlled Oscillator) frequency over a period of time. Based on the curve, we may safely infer that a comparator exists in the AT1846S chip 	
adjusting the frequency of the oscillating signal	In the Programming Guide of the AT1846S chip, as shown below, the range of frequency signal, such as an oscillating signal, may be configured or adjusted based on a selected frequency band.	

according to the comparison result;

3.3 Synthesizer

The frequency synthesizer generates the local oscillator signal. All building blocks are fully without any external components. LO frequency can be programmed through the serial inter MCU. *(How to select frequency band and program LO frequency, refer to the programming g*

Table 5-1 Receiver Characteristics

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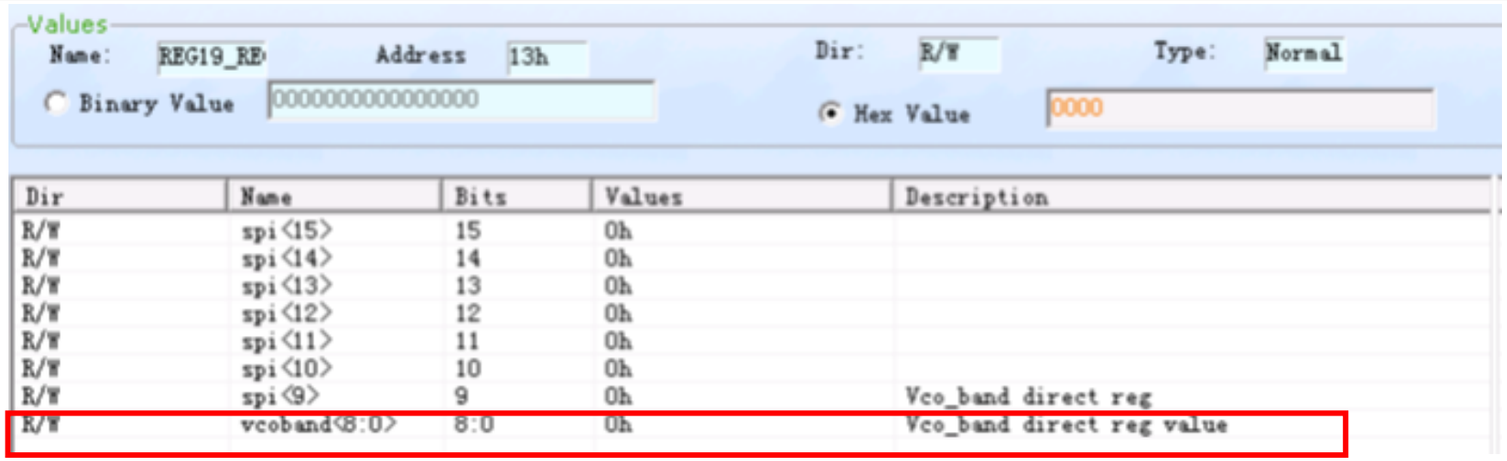
In the Programming Guide of the AT1846S chip, as shown below in the red rectangular box, the oscillating signal is configured or adjusted based on the frequency band <8:0>. The selection of frequency band may be determined according to the comparison result.



Values

Name: REG19_RE Address 13h Dir: R/W Type: Normal

Binary Value 0000000000000000 Hex Value 0000

Dir	Name	Bits	Values	Description
R/W	spi<15>	15	0h	
R/W	spi<14>	14	0h	
R/W	spi<13>	13	0h	
R/W	spi<12>	12	0h	
R/W	spi<11>	11	0h	
R/W	spi<10>	10	0h	
R/W	spi<9>	9	0h	Vco_band direct reg
R/W	vcoband<8:0>	8:0	0h	Vco_band direct reg value

The screenshot in the Programming Guide of the AT1846S chip further indicates frequency signal may be configured or adjusted based on frequency band, such as Freq<29:0>.

1. Setting RF Frequency

Bit	Name	Function
29H[13:0]	freq<29:16>	Freq high value (unit 1khz/16)
2aH[15:0]	freq<15:0>	Freq low value (unit 1khz/16)

Default frequency is 409.7500MHz

Freq<29:0>= Binary (Freq(MHz)*16000)

For example: frequency is 409.75MHz, Freq<29:0>=409.75*16000=6556000=0x640960,so write 29H [15:0] =0x64 and 2aH [15:0] =0x0960.

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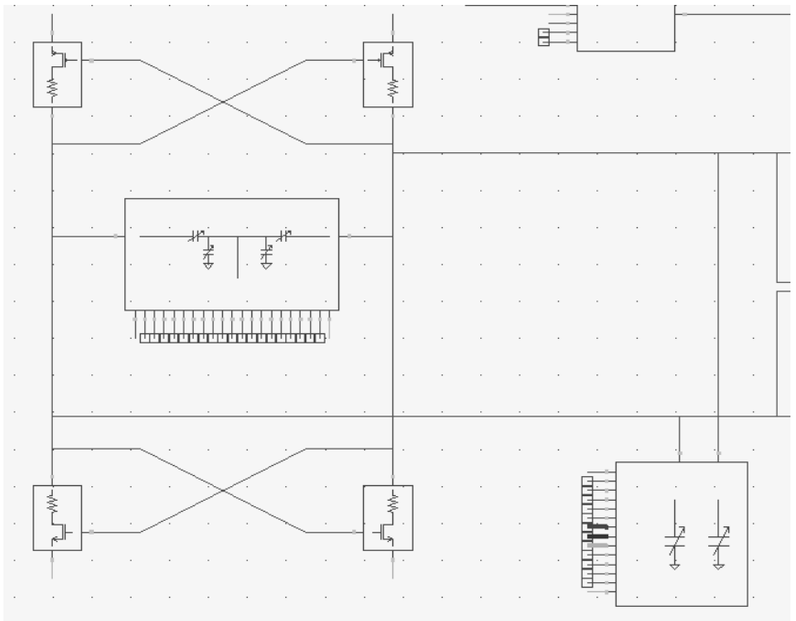
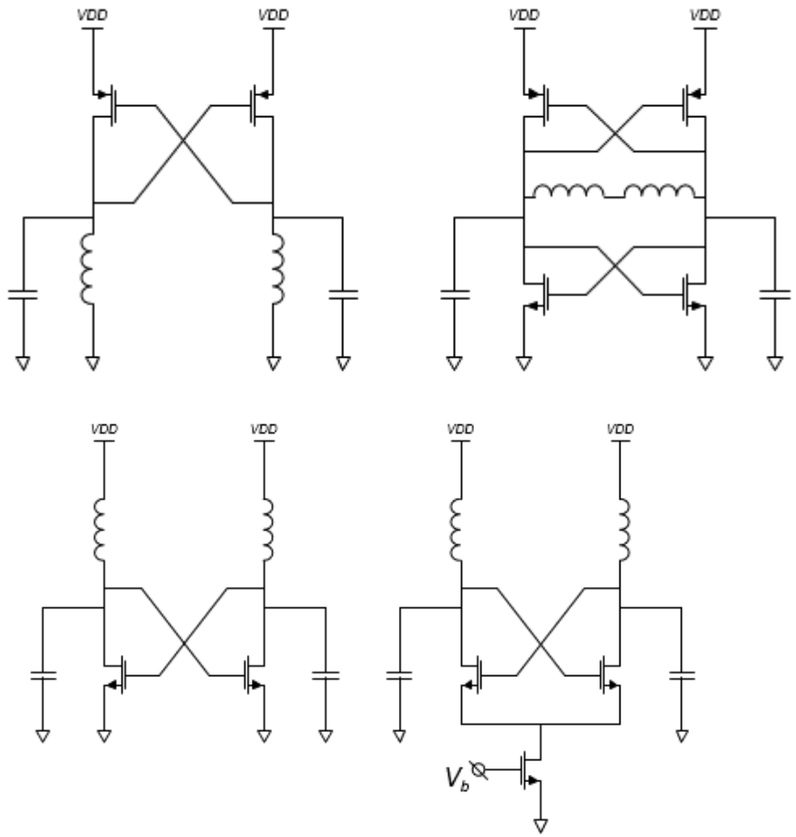
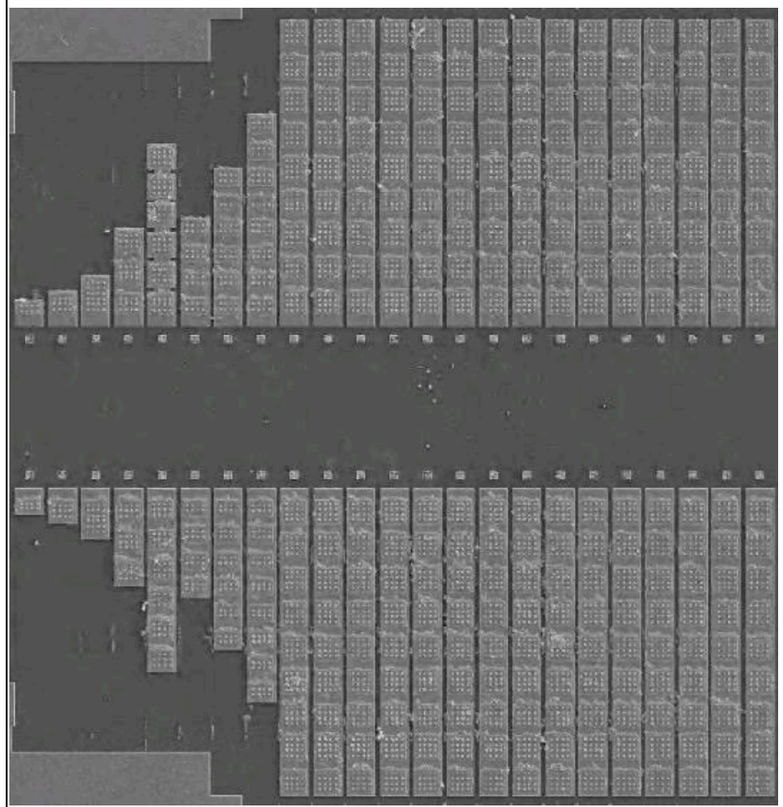
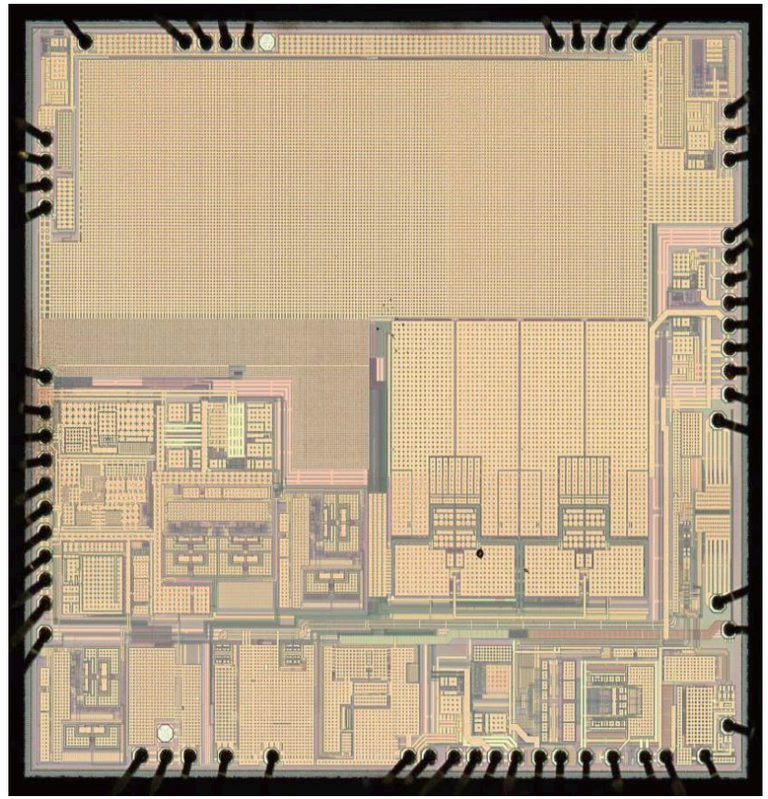
wherein the oscillator comprises a first inductor communicatively coupled to a first capacitor array;	A typical oscillator circuit includes plural energy-storing components, such as capacitors, or inductors, or both. The circuit diagram below shows a circuit of typical oscillators that contains plural capacitors  (e.g., capacitor array) and inductors "."  

Further, as shown below, a capacitor array in the picture to the left is identified from the top view of the AT1846S chip.

The capacitor array in the AT1846S chip:

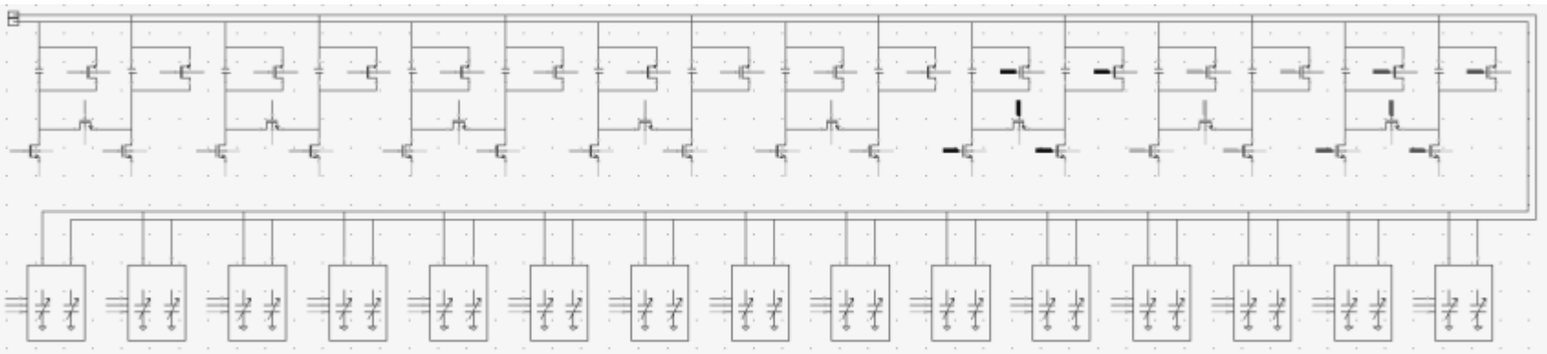


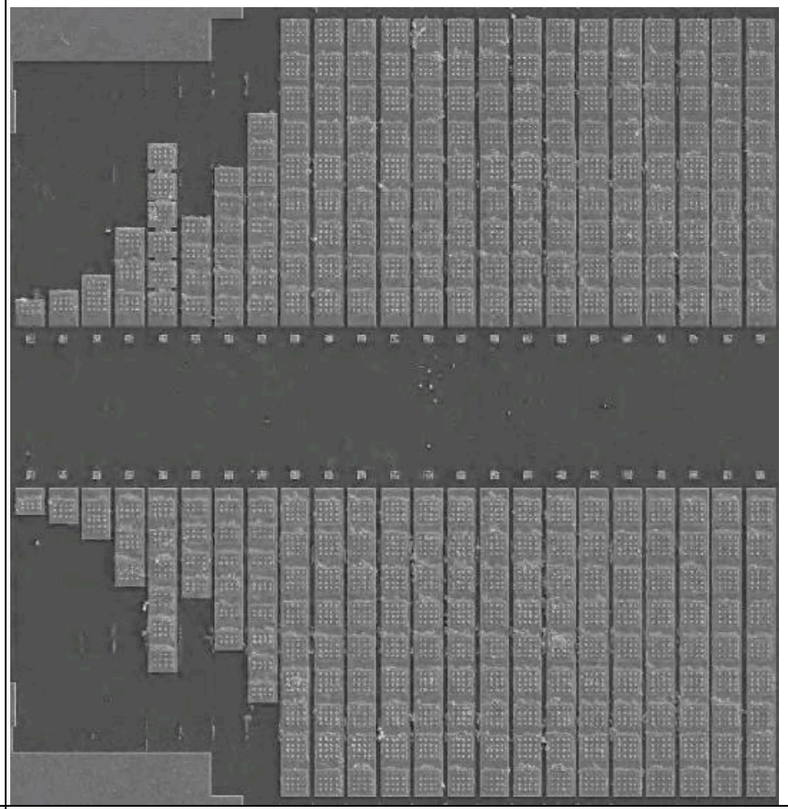
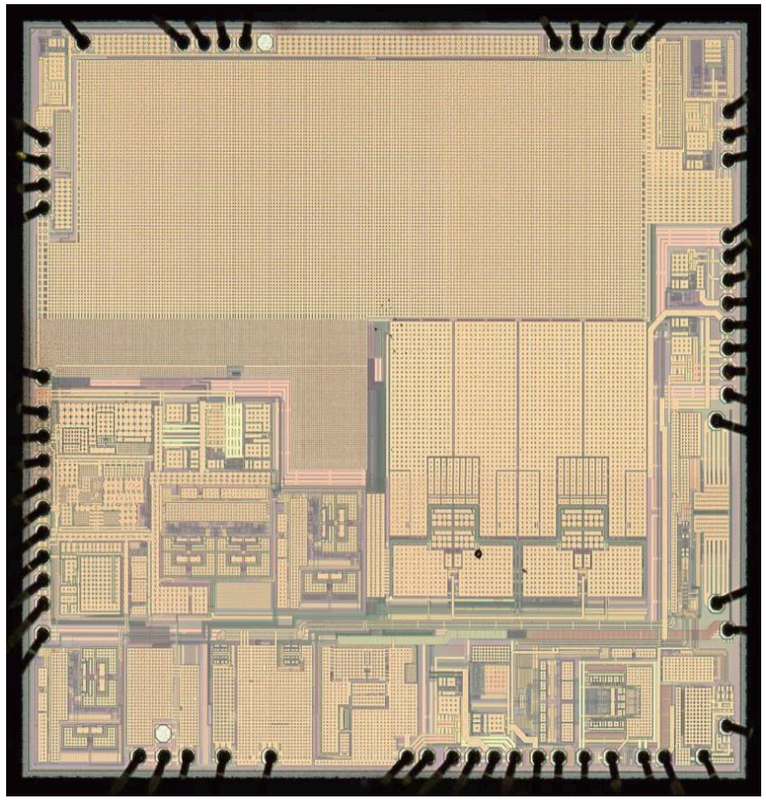
Top view of the AT1846S chip:



obtaining the comparison result;	As discussed above, based on the curve indicating the changes of VCO frequency over a period of time, we may safely infer that a comparator exists in the AT1846S chip. The comparison result is the output of the comparator and may be obtained. A comparator is utilized in the AT1846S chip to generate a comparison result according to a comparison of the first count of the divided signal and the second count of a reference signal. The existence of a comparator may be inferred by testing digital signals in the chip. For example, an aging calibration curve generated by digital signals may be analyzed to infer the existence of a comparator. The screenshot below shows a curve indicating changes of VCO (Voltage-Controlled Oscillator) frequency over a period of time. Based on the curve, we infer that a comparator exists in the AT1846S chip	

		
adjusting the capacitance of the first capacitor array according to the comparison result	Because a capacitor array is identified and is communicatively coupled to the comparator in the AT1846S chip, it may be presumed that the capacitance may be adjusted based on the output (e.g., the comparison result) of the comparator.	

wherein the first capacitor array comprises a plurality of individually switched capacitors,	A typical capacitor array includes a plurality of individually switched capacitors, as shown below.  Further, as shown below, a capacitor array in the picture to the left is identified from the top view of the AT1846S chip.	

	The capacitor array in the AT1846S chip:  Top view of the AT1846S chip: 	
wherein a capacitance of a first capacitor is less than the sum of capacitances of all the other	The graph below shows a LO frequency curve generated by the AT1846S chip below. It may be inferred that the capacitance of the first capacitor is less than the sum of capacitances of all the other capacitors that are less than the first capacitor and the capacitance of the least significant bit of the capacitor array. Otherwise, the curve shall not be smooth and continuous.	

capacitors that are less than the first capacitor and the capacitance of a least significant bit of the capacitor array.